CLAIMS

What is claimed is:

1. A boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline.

2. The boosted memory array of Claim 1, wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline.

3. The boosted memory array of Claim 2, wherein;

said bitline boost enable signal is active only during write operation.

4. The boosted memory array of Claim 2, wherein; said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a second input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

5. The boosted memory array of Claim 4, wherein;

said first and second transistors are NFETS and said supply voltage is ground.

6. The boosted memory array of Claim 4, wherein;

said boosted memory array is on the same silicon chip as a microprocessor.

7. A microprocessor chip, said microprocessor chip comprising:

one or more functional blocks; and

a boosted memory array, said boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline.

8. The microprocessor chip of Claim 7, wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline.

9. The microprocessor chip of Claim 8, wherein;

said bitline boost enable signal is active only during write operation.

10. The microprocessor chip of Claim 9, wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

11. The microprocessor chip of Claim 10, wherein; said first and second transistors are NFETS and said supply voltage is ground.

12. A method for boosting the performance of a memory array comprising:

providing at least one bitline;

coupling at least one memory cell to said at least one bitline;

coupling a bitline booster circuit to said at least one bitline;

coupling a bitline booster circuit bitline boost enable signal input terminal to said bitline booster circuit;

coupling a bitline boost enable signal to said bitline booster circuit bitline boost enable signal input terminal, such that;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline.

13. The method for boosting the performance of a memory array of Claim 12, wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline.

14. The method for boosting the performance of a memory array of Claim 13, wherein;

said bitline boost enable signal is active only during write operation.

15. The method for boosting the performance of a memory array of Claim 14, wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first

transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

16. The method for boosting the performance of a memory array of Claim 15, wherein;

said first and second transistors are NFETS and said supply voltage is ground.

17. The method for boosting the performance of a memory array of Claim 15, wherein;

said boosted memory array is on the same silicon chip as a microprocessor.

18. A method for improving the performance of a microprocessor chip, said method comprising:

providing one or more functional blocks on said microprocessor chip;

providing a boosted memory array, said boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline.

19. The method for improving the performance of a microprocessor chip of Claim 18, wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline.

20. The method for improving the performance of a microprocessor chip of Claim 18, wherein;

said bitline boost enable signal is active only during write operation.

21. The method for improving the performance of a microprocessor chip of Claim 20, wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow

electrode of said second transistor being coupled to said supply voltage.

22. The method for improving the performance of a microprocessor chip of Claim 21, wherein;

said first and second transistors are NFETS and said supply voltage is ground.